Regenerative Frequency Division with a GaAs FET

CHRISTEN RAUSCHER, SENIOR MEMBER, IEEE

Abstract — **The circuit concept to be described accomplishes regenerative frequency division by employing a GaAs FET which is biased near pinchoff. The concept aims at efficient utilization of basic device characteristics, providing well-behaved divider performance and easy circuit designability. This is exemplified with the help of an experimental 16-to-8-GHz divider circuit whose output response is studied for single-tone CW, RF-pulsed, and two-tone CW excitations.**

I. Introduction

FREQUENCY DIVISION is quite essential to a variety of microwave system needs. Among the classic examples are applications involving straight frequency counting, as well as phase-locked loops. Further applications lie in the area of electronic warfare, where the ability of divider circuits to compress bandwidths can be exploited in the processing of wideband signals. Microwave frequency dividers have also been considered for use in FM communications systems, whereby a given signal is subjected to frequency division, amplified, and subsequently restored to the original frequency band with the help of a frequency multiplier. Historically, interest in this scheme was spurred by a need for all-solid-state amplification at a time when available direct amplification using microwave transistors did not yet meet with system requirements.

There have been a number of different microwave frequency divider concepts described in the literature. Each of these individual concepts may be viewed as fitting into either of two basic categories. The first such category comprises circuits that function like digital frequency counters, yielding instantaneous frequency division of a given signal on essentially a cycle-by-cycle basis. High-speed logic circuits, naturally, belong to this group. They are capable of broad-band performance up into the lower microwave frequency range. This first category also includes divider circuits that employ two-terminal and three-terminal transferred-electron devices [1]. By designing the devices to exhibit appropriate transit-time characteristics, traveling domain nucleation can be made to occur only every nth cycle of the incident signal, thereby performing like a frequency counter, but subject to inherent transit-time-related bandwidth constraints.

The second major category contains the regenerative divider circuits whose concept, as illustrated in Fig. 1, has been known for quite some time [2]. The necessary ingredients include amplification, mixing capability, subharmonic feedback, and filtering. In briefly reviewing the basic operation, it is assumed that a signal component at the subharmonic of the incident signal frequency is present initially, either due to noise or input signal transients. This signal is then mixed with the incident signal to produce a lower sideband at the subharmonic which subsequently is filtered out, amplified, and fed back to the mixer. To avoid spurious oscillations, the loop gain must be less than unity in the absence of an injected input signal. With increasing drive level, the mixer contribution to overall loop gain increases accordingly, leading to the buildup of a subharmonic oscillation as the loop gain exceeds unity. This yields an accurately frequency-divided counterpart to the input signal, with the turn-on threshold for the subharmonic oscillation determined by the quiescent loop gain. The regenerative divider process is afflicted, however, with various inherent peculiarities. As will be illustrated, these include partial loss of amplitude information, leading-edge delay for pulsed signals, and confusion if the incident signal contains more than one prominent frequency component.

Early implementations of the regenerative concept have involved discrete components joined together in a circuit resembling the one indicated in Fig. 1. More recently, an implicit realization of this same concept has been reported [3], whereby a pair of varactor diodes is used to simultaneously provide both (parametric) amplification *and* mixing. In the absence of additional means of amplification, the lower bound on the turn-on threshold level remains dictated by varactor and circuit losses. A variation of the same idea is to perform the varactor functions with the nonlinear gate–source capacitances of a pair of MESFET's [4], while utilizing transistor gain for post-amplification of the generated subharmonic signal.

The circuit described in the following also relies on MESFET characteristics to accomplish regenerative frequency division [5]. Emphasis, however, is on achieving an efficient division process by exploiting primarily the transconductance nonlinearity in the vicinity of pinchoff and by directly involving transistor gain in the regenerative process. Within the constraints of maximum available transistor gain, the amount of gain actually utilized is an independent parameter, allowing the turn-on threshold, in principle, to be set at any arbitrary low value.

Manuscript received February 8, 1984; revised June 6, 1984.

The author is with the Dept. of the Navy, Naval Research Laboratory, Code 6851, Washington, D.C. 20375.

0018-9480/84/1100-1461$01.00 ©1984 IEEE

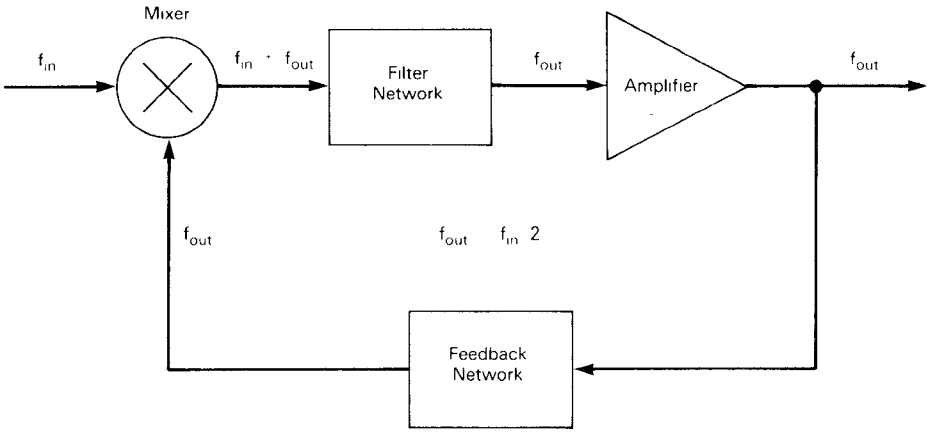

Fig. 1. General concept of regenerative frequency division.

II. The GaAs FET Frequency Divider

The divider circuit investigated in the present context focuses on biasing the transistor slightly above pinchoff where it offers a combination of pronounced quadratic-type transconductance nonlinearity for efficient mixing and multiplying, as well as directional gain. This combination, which is known to yield efficient frequency doubler performance [6], also appears ideally suited for obtaining efficient regenerative frequency division, as the two types of circuits share basic requirements. With reference to Fig. 1, the transistor is thus capable of satisfying both the function of mixing and that of subharmonic amplification, all in one. The transistor merely needs to be augmented by appropriate embedding circuitry to perform the remaining feedback and filtering functions.

A frequency divider of this kind essentially constitutes a circuit designed to oscillate at the subharmonic of the input signal frequency, but with the amount of feedback reduced just enough to prevent actual oscillation from occurring in the absence of an injected signal. Therefore, in principle, any conventional oscillator circuit configuration could be adapted for serving as a frequency divider. A logical choice —and the one studied in the following—is to employ the transistor in common-source configuration as indicated in Fig. 2. The input coupling network is tasked with matching the gate–source port of the transistor to the external signal generator at the input, while simultaneously blocking the internally generated subharmonic signal. Likewise, the output coupling network selectively matches the transistor drain–source port to the external load at the subharmonic frequency, while rejecting other signal components. Parallel-type feedback is used in this instance to support the regenerative process.

Intuitively, there should be little doubt that such a circuit will, indeed, frequency divide. But it is difficult to anticipate how well this type of divider will actually behave in reality. Answers have thus been sought with the help of an experimental GaAs FET frequency halver, accommodating input signals at frequencies around 16 GHz. A schematic of this circuit is shown in Fig. 3. The values of the various circuit parameters are derived by first designing the circuit to be on the verge of oscillation at the subharmonic frequency of 8 GHz, employing established techniques [7], and then reducing the effective amplitude of the device-external feedback signal by 3 dB to maintain a conservative safeguard against spurious oscillations. This defines the subharmonic matching conditions at the gate–source port and the drain–source port of the transistor, as well as the drain-to-source subharmonic feedback. The input and output coupling networks reflect these constraints, while simultaneously performing the blocking and matching functions at the incident signal frequency and its subharmonic, as outlined earlier. The assignments for the individual circuit elements are readily apparent from the parameter values summarized in the figure caption.

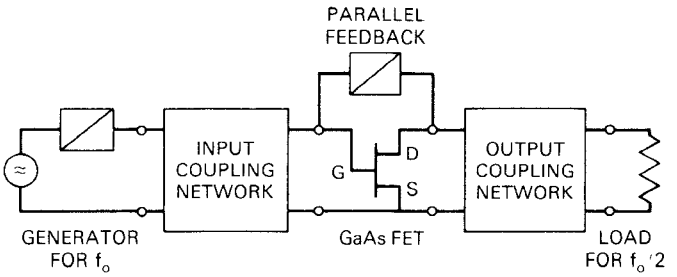

Fig. 2. Frequency divider concept with GaAs FET in common-source configuration.

The actual 16-to-8-GHz divider circuit, implemented in microstrip on a 0.25-mm-thick fiberglass-reinforced teflon substrate, is depicted in Fig. 4. The transistor used in this experiment is one cell of an Avantek M110 GaAs FET with a gate length of 0.5 μm, a gate width of 375 μm, and a pinch-off voltage of -2.9 V. The drain–source and gate–source dc-bias conditions are $V_{DS} = +3.0$ and $V_{GS} = -2.6$ V, respectively. Subharmonic feedback is controlled by a miniature 5-nH air coil inductor and a 5-pF silicon-nitride blocking capacitor connected in series between drain and gate terminals. The inductor consists of seven turns of gold wire with an approximate coil diameter of 300 μm.

III. Experimental Results

In order to obtain quantitative information on GaAs FET divider performance, three different test cases have been selected which are believed to be representative of typical situations encountered in practice. These test cases comprise subjecting the circuit to single-frequency CW excitation, single-frequency pulsed excitation, and two-tone

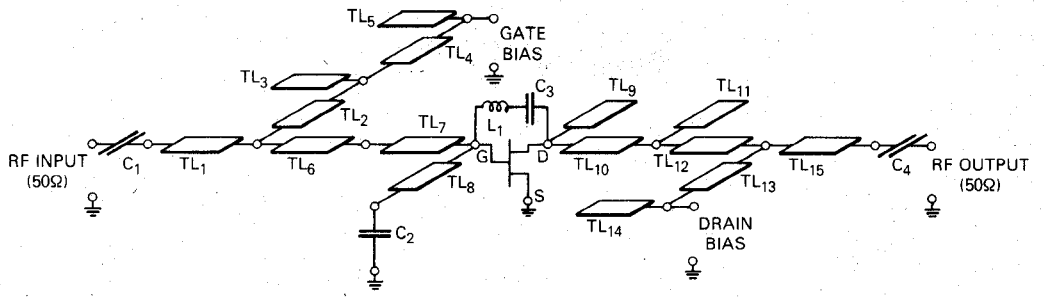

Fig. 3 Schematic circuit diagram of experimental 16-to-8-GHz GaAs FET frequency divider using one cell of a half-micron Avantek M110 device biased near pinchoff. The values of characteristic impedance Z_o and electrical length θ at 16 GHz of the various transmission line elements are:

TL_1: $Z_o = 95\Omega$, $\theta = 33.5°$
TL_2: $Z_o = 95\Omega$, $\theta = 90°$
TL_3: $Z_o = 95\Omega$, $\theta = 90°$
TL_4: $Z_o = 95\Omega$, $\theta = 180°$
TL_5: $Z_o = 40\Omega$, $\theta = 180°$
TL_6: $Z_o = 95\Omega$, $\theta = 56.5°$
TL_7: $Z_o = 42\Omega$, $\theta = 75°$
TL_8: $Z_o = 51\Omega$, $\theta = 71°$
TL_9: $Z_o = 80\Omega$, $\theta = 43°$
TL_{10}: $Z_o = 70\Omega$, $\theta = 90°$
TL_{11}: $Z_o = 80\Omega$, $\theta = 90°$
TL_{12}: $Z_o = 80\Omega$, $\theta = 130°$
TL_{13}: $Z_o = 95\Omega$, $\theta = 180°$
TL_{14}: $Zo = 40\Omega$, $\theta = 180°$
TL_{15}: $Z_o = 42\Omega$, $\theta = 180°$.

The values of the lumped elements are:

$$C_1 = C_2 = C_4 = 20 \text{ pF}$$
$$C_3 = 5 \text{ pF}$$
$$L_1 = 5 \text{ nH}.$$

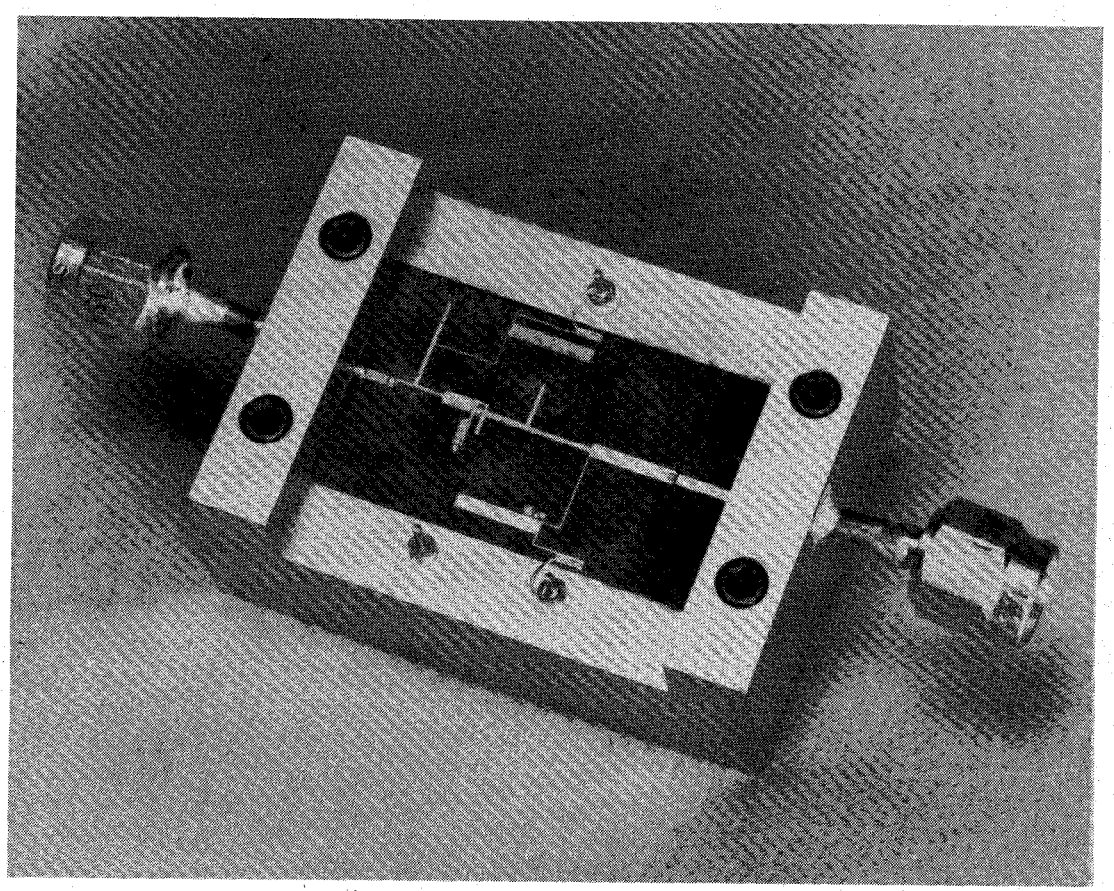

Fig. 4. GaAs FET 16-to-8-GHz frequency divider.

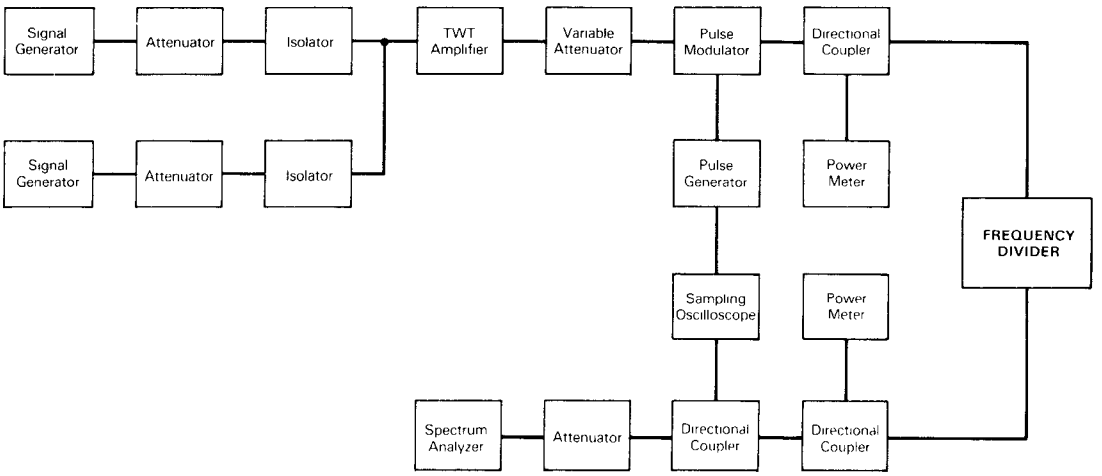

Fig. 5. Block diagram of a setup for measuring frequency divider performance.

CW excitation. The set-up shown in Fig. 5 was used to carry out the various measurements.

A. Single-Frequency CW Operation

The first series of experiments involves the response of the divider circuit to an incident 16.0-GHz CW signal, resulting in a frequency-halved output signal at 8.0 GHz. Measured output power as a function of incident drive level and dc gate–source bias voltage is plotted in Fig. 6. As might be expected, the gate–source bias voltage has a direct effect on the turn-on threshold—the incident power level that must be exceeded before the regenerative process can start up. The nominal design with $V_{GS} = -2.6$ V offers the highest sensitivity with a threshold level of 6.5 dBm. It may be recalled, thereby, that the present circuit configuration would readily permit the threshold level to be reduced to any arbitrary low level through appropriate adjustment of the transistor contribution to overall loop gain. The need to safeguard against spurious oscillations imposes a practical lower limit on threshold level, with appropriate safety margins to be maintained over the entire temperature operating range. Although temperature effects have not been specifically addressed in the present context, they may be estimated based on the bias voltage dependence of divider performance given in Fig. 6, and on the general knowledge of how principal transistor characteristics are apt to change with temperature. Toward the upper end of the input power scale, the output response levels off as the subharmonic oscillation approaches saturation. In between these two extremes, there is a rather limited range where the divider response can be considered reasonably linear. However, the limited dynamic range, which results in a partial loss of original amplitude information, is not specific to the GaAs FET divider, but is a characteristic of the regenerative process itself. Fig. 7 provides further illustration, where the results obtained under the nominal bias conditions have been replotted in terms of conversion efficiency (gain) as a function of input drive level. Also shown in Fig. 7 is the dc drain–source current of the transistor which increases with drive level due to the rectifying action associated with operation in the vicinity of pinchoff.

Rather than aim for specific performance goals, the main objective of this study is to evaluate basic characteristics of the proposed GaAs FET divider circuit. In support of this objective, excess circuit complexity has been intentionally avoided by allowing the bandwidth aspect to be excluded from consideration. As conveyed by the solid-line curve in Fig. 8, the experimental circuit, nonetheless, exhibits a 3-dB threshold bandwidth of approximately 600 MHz relative to the input signal when operating at the nominal gate bias voltage of $V_{GS} = -2.6$V. Fig. 8 also indicates how the threshold response changes when the gate bias voltage is permitted to deviate from its nominal value. In this context, it is worth noting that the threshold response of the GaAs FET divider circuit did not show any signs of hysteresis effects versus drive level, such as have been observed in varactor dividers [3]. Even though verified for the full range of frequencies and gate bias voltages considered in the experiment, the absence of hysteresis effects does not necessarily imply, however, that such effects cannot be reproduced in GaAs FET dividers under special circumstances.

B. Single-Frequency Pulsed Operation

The second series of measurements investigates the response of the divider circuit to pulsed signals of varying amplitudes. One characteristic the present circuit shares with all regenerative frequency dividers is the time delay the leading edge of an RF pulse experiences in the division process. This corresponds to the time it takes the subharmonic signal to build up from noise. The time delay is influenced by such factors as effective circuit-Q and overall loop gain at the subharmonic.

This effect is demonstrated by applying a pulsed 16.0-GHz test signal of 200-ns pulse duration to the input of the circuit, with the transistor again biased at its nominal operating point. The incident pulses are generated with the help of a high-speed pulse modulator (Fig. 5). A representative sampling oscillogram of an incident pulse is shown in Fig. 9, with the shape of the pulse envelope found to be independent of pulse amplitude for all practical purposes. Fig. 10 depicts the 8.0-GHz frequency-divided response for a range of pulse amplitudes. It is thereby

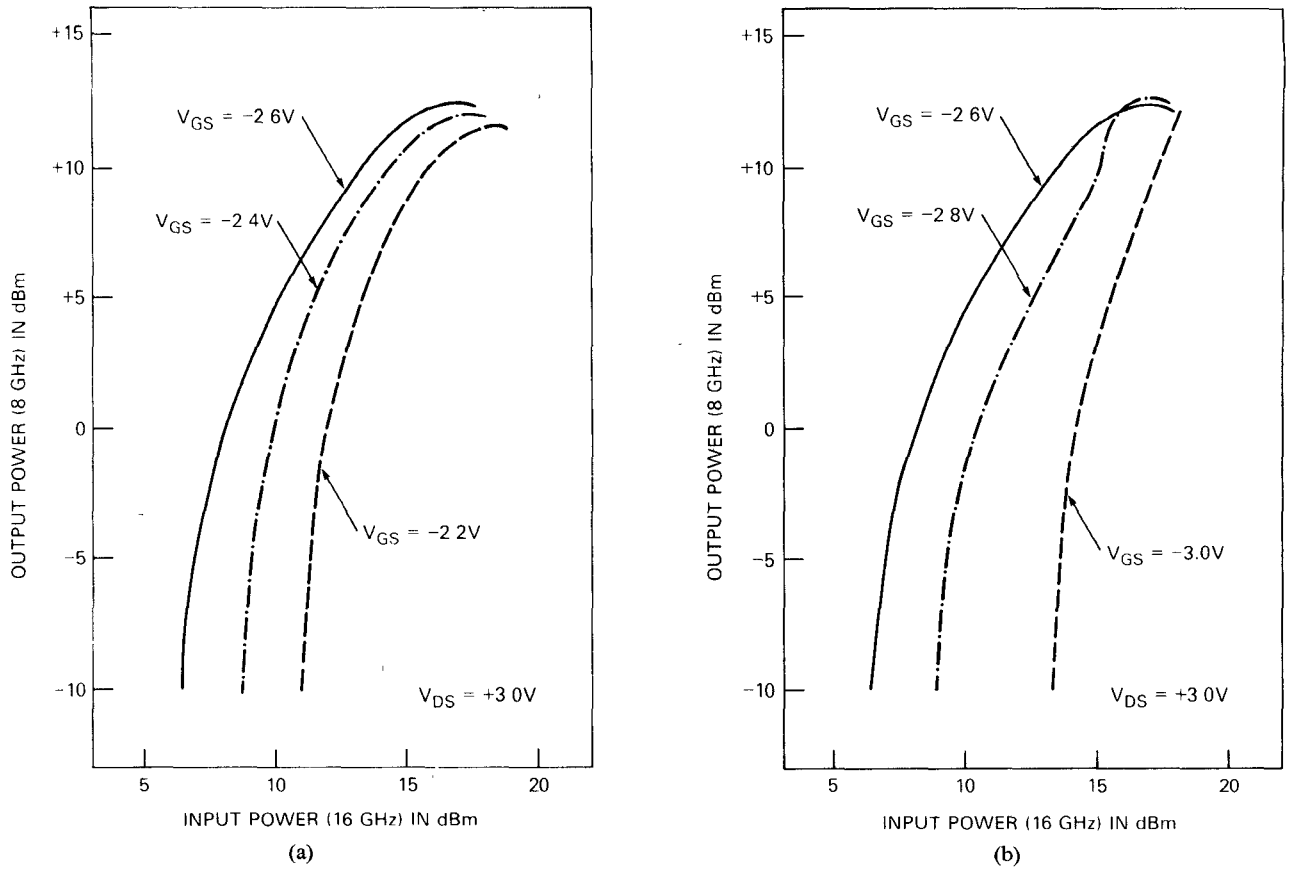

Fig. 6. (a) and (b). Measured 8-GHz subharmonic output power as a function of 16-GHz input drive level and dc gate–source bias voltage.

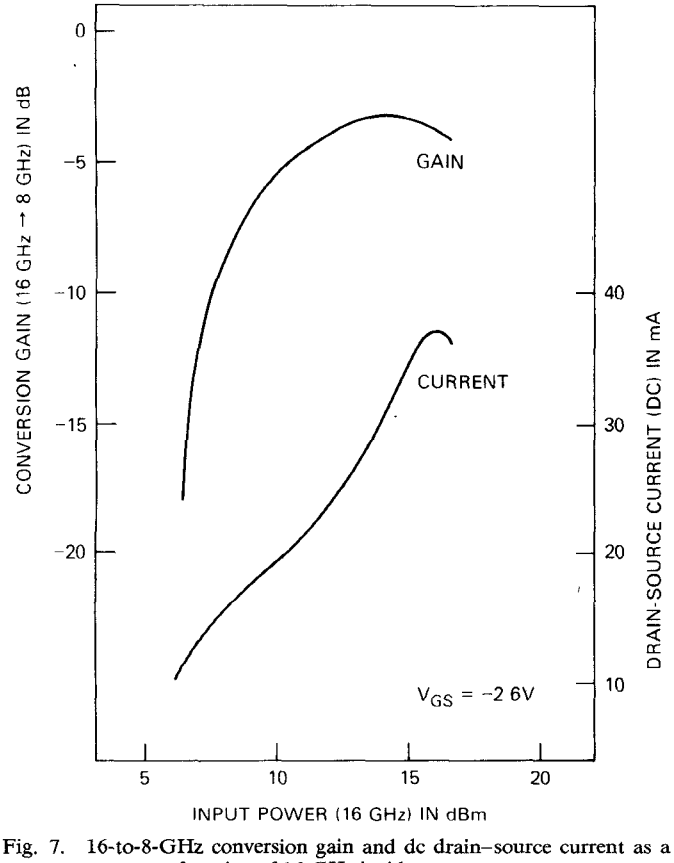

Fig. 7. 16-to-8-GHz conversion gain and dc drain–source current as a function of 16-GHz incident power.

apparent how the leading edge delay decreases as the output signal responds to increasing 16.0-GHz drive levels. This should be expected, based on the observation that increasing input drive levels directly translate into increasing effective loop gains. With the exception of the inherent leading-edge delay phenomenon, the output response is otherwise well behaved, showing similar characteristics over the full operating frequency range. The response does not exhibit, for instance, the kind of amplitude fluctuations during the designated steady-state portion of the output pulse that have been occasionally observed in regenerative varactor frequency dividers [8]. Within the steady-state domain, the GaAs FET divider actually operates as if it were responding to true CW excitation, permitting the relationship between peak output power and peak input power to be directly acquired from CW conversion gain information, such as that contained in Figs. 6 and 7.

C. Two-Tone CW Excitation

The third test case addresses the situation where incident signals are present at more than just one frequency. Ideally, a divider circuit would be expected to translate any given input spectrum to the subharmonic frequency band by frequency dividing each individual spectral component in a similar fashion. In special situations this may be readily achieved—such as when dealing with a class of FM input signals [9], [10]. For the most part, however, the regenerative divider is apt to single out the dominant

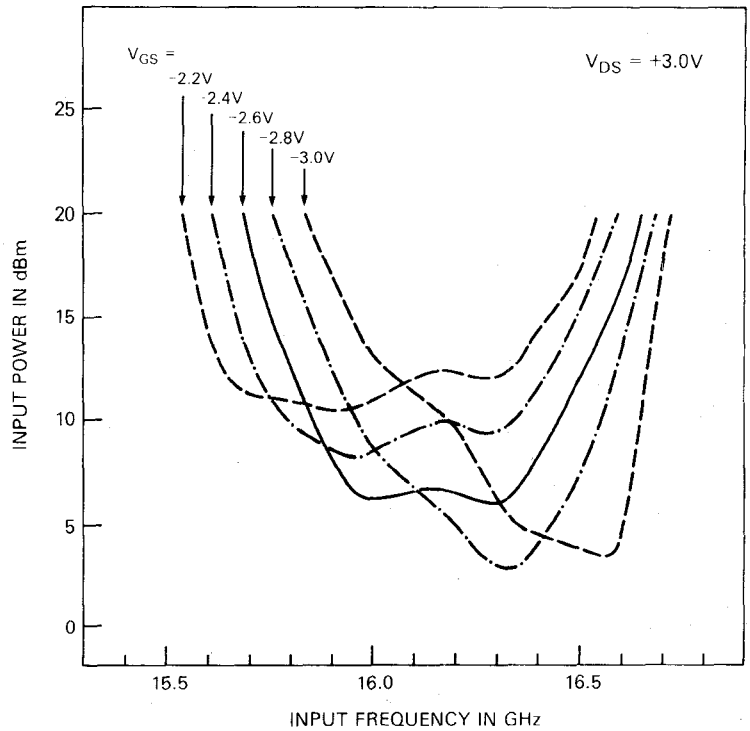

Fig. 8. Turn-on threshold response as a function of input frequency and dc gate–source bias voltage.

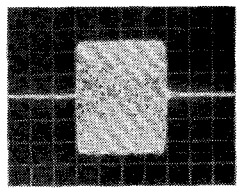

Fig. 9. Incident 16-GHz pulse of 200-ns duration. Time scale: 50 ns per division.

component of the input spectrum and only subject it to actual frequency division, while simply down-converting the rest of the spectrum through intermodulation. Depending on the type of spectrum involved, this can lead to confusion in interpreting the output response.

To investigate divider performance under multiple-signal excitation, a two-tone input signal is used, involving a primary fixed-amplitude CW component at 16.0 GHz and a secondary component whose amplitude or frequency is varied, depending on the case. In the measurement set-up (Fig. 5), special care is taken to reduce to negligible levels all intermodulation products stemming from interaction of the input generators between themselves. This is verified in Fig. 11, where the intermodulation products are shown to be at least 40 dB below each of the two +16 dBm primary signal components. These correspond to the maximum saturating drive levels used in the experiments.

The series of output spectra given in Fig. 12 illustrates the divider response to an incident signal containing two components of variable relative amplitudes. The signal strength of the 16.0-GHz primary component, thereby, is

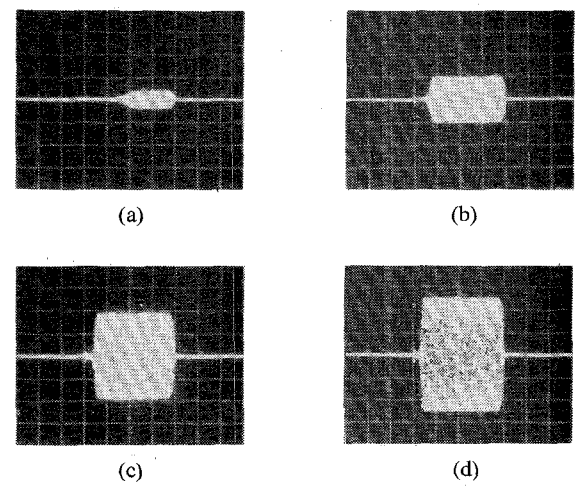

Fig. 10. 8-GHz pulsed output response for 16-GHz incident peak power levels of: (a) +7 dBm, (b) +10 dBm, (c) +13 dBm, and (d) +16 dBm. Time scale: 50 ns per division.

held constant at +10 dBm, while the power of the 16.1-GHz secondary signal is increased from zero to 20 mW (+13 dBm). Fig. 12(a) shows the clean 8-GHz divider response to the 16.0-GHz primary signal with no secondary input signal present. With increasing strength of the secondary input signal, additional lines begin to appear in the output spectrum. Unlike the principal output line at 8.0 GHz, these additional lines are not subharmonically related to the input spectrum. They are merely the product of intermodulation among the various applied and generated signals present, which is evidenced by the 100-MHz output

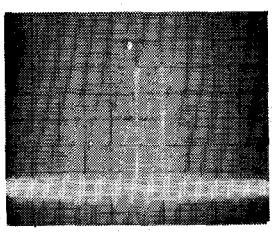

Fig. 11. Spectrum of incident two-tone CW signal with each tone set at +16 dBm. Frequency scale, horizontal: 100 MHz per division centered at 16 GHz. Amplitude scale, vertical: 10 dB per division.

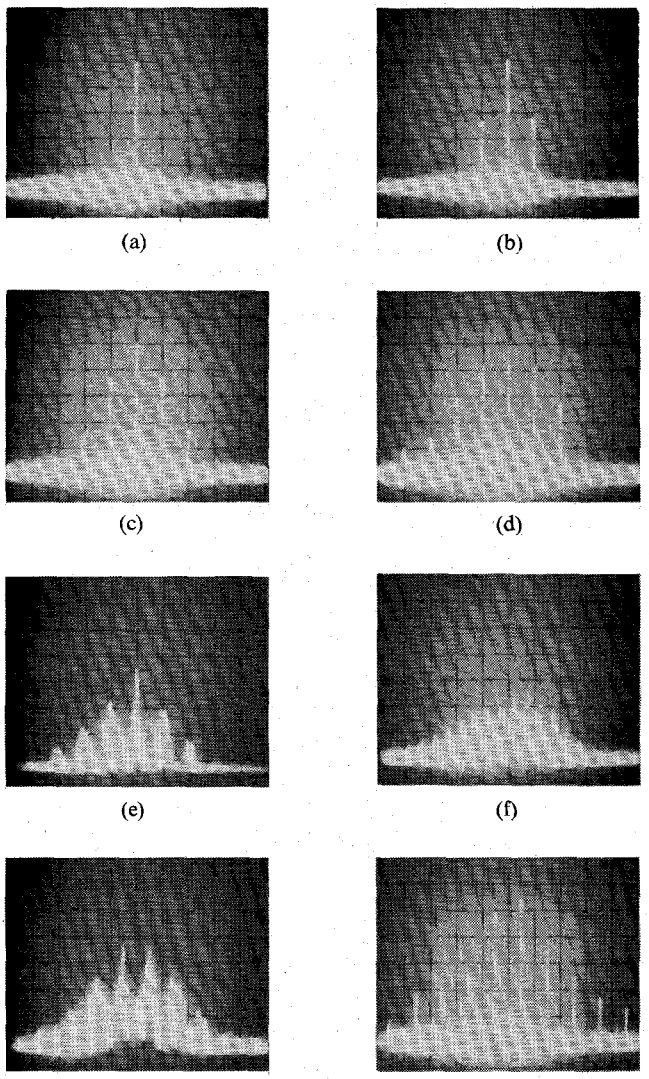

Fig. 12. Output spectra for two-tone CW excitations consisting of a fixed +10 dBm signal at 16.0 GHz and a second signal at 16.1 GHz whose amplitude is varied according to: (a) 0 mW (b) −10 dBm, (c) 0 dBm, (d) +7 dBm, (e) +9 dBm, (f) +10 dBm, (g) +11 dBm, and (h) +13 dBm. Frequency scale, horizontal: 100 MHz per division centered at 8.0 GHz. Amplitude scale, vertical: 10 dB per division.

line spacing equaling the original 100-MHz separation of the two input tones.

As the two input tones approach one another in amplitude and the 16.1-GHz component begins to challenge the dominance of the 16.0-GHz component, the output response becomes very noisy. This is especially evident in the

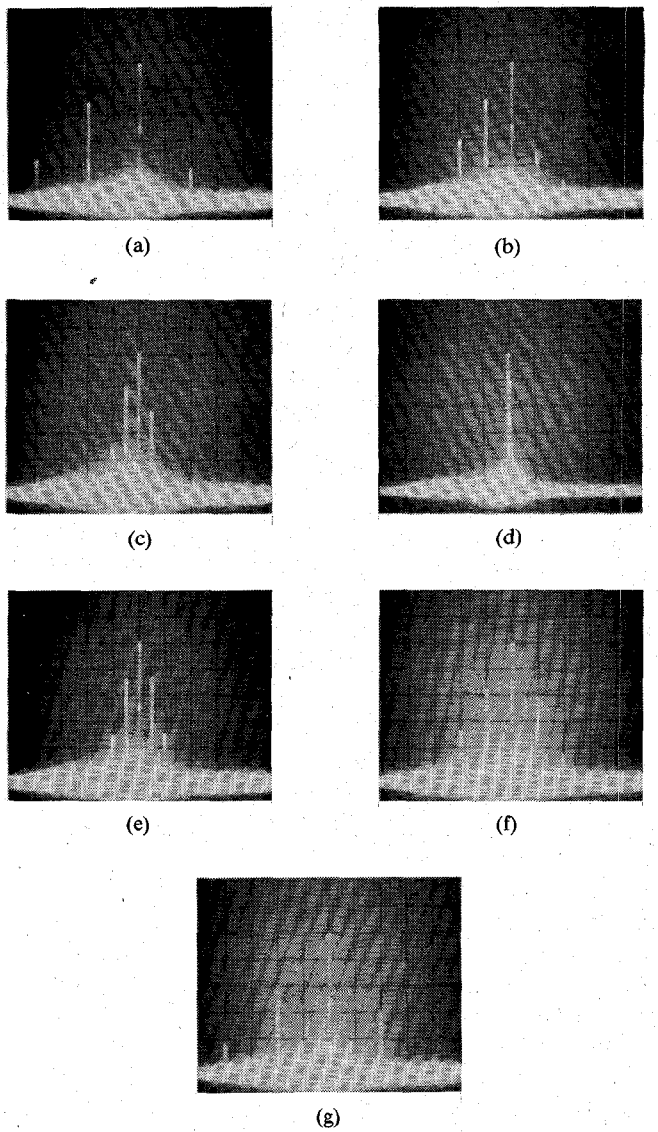

Fig. 13. Output spectra for two-tone CW excitations comprising a fixed +10 dBm signal at 16.0 GHz and a second 0-dBm constant-amplitude signal whose frequency is varied according to: (a) 15.6 GHz, (b) 15.8 GHz, (c) 15.9 GHz, (d) 16.0 GHz, (e) 16.1 GHz, (f) 16.2 GHz, and (g) 16.4 GHz. Frequency scale, horizontal: 200 MHz per division centered at 8.0 GHz. Amplitude scale, vertical: 10 dB per division.

case shown in Fig. 12(f) where, for equal amplitudes of the two tones, the circuit ceases to engage in any meaningful frequency divider operation. The seemingly anomalous behavior can be explained as a direct consequence of the injection-locked oscillator characteristics of the regenerative concept itself, as multiple injected signals interfere with establishing a defined and stable state of oscillation.

Then, as the amplitude of the 16.1-GHz signal component is increased even further, it takes over the lead, resulting in the generation of a subharmonic response at 8.05 GHz. This is apparent in Fig. 12(h), where the positions of the various spectral lines have been shifted by 50 MHz, with the most prominent line representing the subharmonic. The spacing between the lines remains 100 MHz, indicating that the auxiliary lines grouped around the subharmonic signal continue to be the result of intermodulation rather than divider action.

The basic observations relating to the previous example are not specifically linked to the 100-MHz separation between the two incident tones. Indeed, this reflects a quite arbitrary choice, constrained only by the requirement that both signal components fall comfortably within the threshold bandwidth of the circuit. As a further illustration, Fig. 13 presents an additional set of output spectra, this time involving variable spacing between the two incident tones. The primary input signal component is again set at 16.0 GHz with a +10-dBm associated power level. A fixed-amplitude 0-dBm signal is used as the secondary input component, with its frequency allowed to vary from 15.6 to 16.4 GHz. The pictures suggest that the separation between the input tones does not have a major impact on the basic performance characteristics of the divider circuit. This pertains, incidentally, also to the equal-amplitude phenomenon discussed above. Naturally, the spectral composition of the output response does exhibit some degree of variation across the band, which is to be expected when considering the inherent bandwidth constraints of the test circuit as well as its highly nonlinear properties.

IV. Summary and Conclusions

The present study is aimed as demonstrating an effective regenerative microwave frequency divider concept in which a GaAs FET is employed to satisfy both the amplifying and the mixing requirements of the regenerative process. This is achieved by biasing the transistor slightly above pinchoff, where it exhibits both gain and pronounced transconductance nonlinearity. With emphasis on investigating basic performance characteristics, the question of maximizing bandwidth was left aside. The rather simple experimental circuit, nevertheless, showed a 3-dB threshold bandwidth of approximately 600 MHz, relative to the input—in itself, sufficient for several phase-locked loop situations. The implementation of wider bandwidths of up to an octave, which might involve a balanced configuration to ease separation of input and output signals, is chiefly a matter of applying established broad-band matching techniques rather than a matter of challenging some fundamental limitation. The frequencies of the input test signal were hence all chosen at or in the immediate vicinity of the nominal design input frequency of 16 GHz, yielding output signal responses around 8 GHz.

The GaAs FET divider proved to be very well behaved under both CW and RF pulsed excitations. It did not exhibit threshold hysteresis effects under CW excitation or amplitude fluctuations in its pulsed response, such as have been observed in other types of regenerative divider circuits. The concept also offers the convenience of permitting the turn-on threshold to be set arbitrarily low, as the presence of the transistor allows, in effect, overall loop gain to be chosen as an independent design parameter. The GaAs FET divider naturally remains subject to the various behavioral peculiarities typical of regenerative dividers as a whole, exemplified in the experiments by the observations regarding limited dynamic range, leading-pulse-edge delay, and response to multiple signal excitation. Despite those impeding factors, regenerative frequency dividers can be quite useful in a variety of systems applications. It is believed that the divider circuit presented here offers an attractive option for such applications, based on its conceptual simplicity, easy designability, and well-disposed performance characteristics.

Acknowledgment

The author wishes to thank H. E. Heddings for his assistance in assembling the test circuit.

References

[1] L. C. Upadhyayula and S. Y. Narayan, "Microwave frequency dividers," *RCA Review*, vol. 34, pp. 595–607, Dec. 1973.
[2] R. L. Miller, "Fractional frequency generation utilizing regenerative modulation," *Proc. IRE*, vol. 37, pp. 446–456, July 1939.
[3] R. G. Harrison, "A broad-band frequency divider using microwave varactors," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-25, pp. 1055–1059, Dec. 1977.
[4] W. D. Cornish, "Wideband MESFET microwave frequency divider," U.S. Patent 4, 327, 343, Apr. 1982.
[5] C. Rauscher, "A 16 GHz GaAs FET frequency divider," in *1983 IEEE MTT Soc. Int. Microwave Symp. Dig.*, June 1983, pp. 349–351.
[6] C. Rauscher, "High-frequency doubler operation of GaAs field-effect transistors," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-31, pp. 462–473, June 1983.
[7] C. Rauscher, "Large-signal technique for designing single-frequency and voltage-controlled GaAs FET oscillators," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-29, pp. 293–304, Apr. 1981.
[8] R. D. Gurney, "Analysis of a varactor frequency divider," unpublished.
[9] G. Immovilli and G. Mantovani, "Analysis of a Miller frequency divider by two in view of applications to wideband FM signals," *Alta Frequenza*, vol. 17, pp. 313–326, Nov. 1973.
[10] S. V. Ahamed, J. C. Irvin, and H. Seidel, "Study and fabrication of a frequency divider-multiplier scheme for high-efficiency microwave power," *IEEE Trans. Commun. Tech.*, vol. COM-24, pp. 243–249, Feb. 1976.

Christen Rauscher (S'73–M'75–SM'81) was born in Boston, MA, on November 4, 1944. He received the diploma in electrical engineering and the Ph.D. degree in 1969 and 1975, respectively, both from the Swiss Federal Institute of Technology, Zurich, Switzerland.

From 1969 to 1976, he was employed as an Assistant and Research Associate at the Microwave Laboratory of the Swiss Federal Institute of Technology, where he conducted research on computer-aided tolerance optimization of microwave active circuits and on IMPATT power amplifiers. He held a Post-Doctoral Fellowship from the Swiss National Science Foundation from 1976 to 1978. He spent this time at Cornell University, Ithaca, NY, and the Naval Research Laboratory, Washington, D.C., investigating the nonlinear behavior of GaAs MESFET's. Since 1978, he has been employed at the Naval Research Laboratory. Washington, D.C., engaged in research on microwave and millimeter-wave nonlinear circuits.